Cadence Rtl Compiler User Manual

Lightweight Cryptography for Security and PrivacyASIC & EDADomain Specific High-Level Synthesis for Cryptographic WorkloadsTransaction-Level Power ModelingThe Verilog® Hardware Description LanguageDigital Logic Design Using VerilogEDA for IC Implementation, Circuit Design, and Process TechnologyFPGAs for Software ProgrammersLanguages for Digital Embedded SystemsThe Designer's Guide to Verilog-AMSConstraining Designs for Synthesis and Timing AnalysisTwelfth International Conference on VLSI DesignElectronic DesignSystemVerilog for VerificationHandbook of Research on Advanced Hybrid Intelligent Techniques and ApplicationsTcl and the Tk ToolkitMIPS Microprocessor Simulation Using Cadence NC-Verilog Simulation EnvironmentVerilog HDLVerification Methodology Manual for SystemVerilogThe Design Warrior's Guide to FPGAsEDNASIC/SoC Functional Design VerificationVerilog — 2001Electronic BusinessReuse Methodology ManualEnergy-Efficient Communication ProcessorsSynthesis Methodology for Built-in At-speed Testing17th IEEE VLSI Test SymposiumThe ASIC HandbookLogic Synthesis Using Synopsys®Advanced ASIC Chip SynthesisSystem-on-a-Chip VerificationAdvanced ASIC Chip SynthesisFunctional Design Errors in Digital CircuitsVHDL Programming with Advanced TopicsThe Designer's Guide to Spice and Spectre®Digital VLSI Chip Design with Cadence and Synopsys CAD ToolsImplementation of

Asynchronous Interface ASIC Flow (RTL-to-GDSII) Using Cadence and Synopsys ToolsFPGA Radio Frequency Identification: Security and Privacy Issues

Lightweight Cryptography for Security and Privacy

The proceedings of the January 1999 conference consist of 103 papers, 11 talks, and six tutorials. The papers are grouped under the headings of TCAD to ECAD, low power, testing, co-design and synthesis, analog design, multi-valued logic, verification, digital signal processor (DSP), logic synthesis,

ASIC & EDA

This book is designed to serve as a hands-on professional reference with additional utility as a textbook for upper undergraduate and some graduate courses in digital logic design. This book is organized in such a way that that it can describe a number of RTL design scenarios, from simple to complex. The book constructs the logic design story from the fundamentals of logic design to advanced RTL design concepts. Keeping in view the importance of miniaturization today, the book gives practical information on the issues with ASIC RTL design and how to overcome these concerns. It clearly explains how to write an efficient RTL code and how to improve design performance. The book also describes advanced RTL design concepts such as low-power design, multiple clock-domain design, and SOC-based

design. The practical orientation of the book makes it ideal for training programs for practicing design engineers and for short-term vocational programs. The contents of the book will also make it a useful read for students and hobbyists.

Domain Specific High-Level Synthesis for Cryptographic Workloads

Transaction-Level Power Modeling

This book serves as a hands-on guide to timing constraints in integrated circuit design. Readers will learn to maximize performance of their IC designs, by specifying timing requirements correctly. Coverage includes key aspects of the design flow impacted by timing constraints, including synthesis, static timing analysis and placement and routing. Concepts needed for specifying timing requirements are explained in detail and then applied to specific stages in the design flow, all within the context of Synopsys Design Constraints (SDC), the industry-leading format for specifying constraints.

The Verilog® Hardware Description Language

Silicon technology now allows us to build chips consisting of tens of millions of transistors. This technology not only promises new levels of system integration onto a single chip, but also presents significant challenges to the chip designer. As a

result, many ASIC developers and silicon vendors are re-examining their design methodologies, searching for ways to make effective use of the huge numbers of gates now available. These designers see current design tools and methodologies as inadequate for developing million-gate ASICs from scratch. There is considerable pressure to keep design team size and design schedules constant even as design complexities grow. Tools are not providing the productivity gains required to keep pace with the increasing gate counts available from deep submicron technology. Design reuse - the use of pre-designed and pre-verified cores - is the most promising opportunity to bridge the gap between available gate-count and designer productivity. Reuse Methodology Manual for System-On-A-Chip Designs, Second Edition outlines an effective methodology for creating reusable designs for use in a System-on-a-Chip (SoC) design methodology. Silicon and tool technologies move so quickly that no single methodology can provide a permanent solution to this highly dynamic problem. Instead, this manual is an attempt to capture and incrementally improve on current best practices in the industry, and to give a coherent, integrated view of the design process. Reuse Methodology Manual for System-On-A-Chip Designs, Second Edition will be updated on a regular basis as a result of changing technology and improved insight into the problems of design reuse and its role in producing high-quality SoC designs.

Digital Logic Design Using Verilog

EDA for IC Implementation, Circuit Design, and Process Technology

This book describes a new design approach for energy-efficient, Domain-Specific Instruction set Processor (DSIP) architectures for the wireless baseband domain. The innovative techniques presented enable co-design of algorithms, architectures and technology, for efficient implementation of the most advanced technologies. To demonstrate the feasibility of the author's design approach, case studies are included for crucial functionality of advanced wireless systems with increased computational performance, flexibility and reusability. Designers using this approach will benefit from reduced development/product costs and greater scalability to future process technology nodes.

FPGAs for Software Programmers

Advanced ASIC Chip Synthesis: Using Synopsys® Design Compiler® and PrimeTime® describes the advanced concepts and techniques used for ASIC chip synthesis, formal verification and static timing analysis, using the Synopsys suite of tools. In addition, the entire ASIC design flow methodology targeted for VDSM (Very-Deep-Sub-Micron) technologies is covered in detail. The emphasis of this book is on real-time application of Synopsys tools used to combat various problems seen at VDSM geometries. Readers will be exposed to an effective design methodology for handling complex, sub-micron ASIC designs. Significance is placed on HDL coding

styles, synthesis and optimization, dynamic simulation, formal verification, DFT scan insertion, links to layout, and static timing analysis. At each step, problems related to each phase of the design flow are identified, with solutions and work-arounds described in detail. In addition, crucial issues related to layout, which includes clock tree synthesis and back-end integration (links to layout) are also discussed at length. Furthermore, the book contains in-depth discussions on the basics of Synopsys technology libraries and HDL coding styles, targeted towards optimal synthesis solutions. Advanced ASIC Chip Synthesis: Using Synopsys® Design Compiler® and PrimeTime® is intended for anyone who is involved in the ASIC design methodology, starting from RTL synthesis to final tape-out. Target audiences for this book are practicing ASIC design engineers and graduate students undertaking advanced courses in ASIC chip design and DFT techniques. From the Foreword: `This book, written by Himanshu Bhatnagar, provides a comprehensive overview of the ASIC design flow targeted for VDSM technologies using the Synopsis suite of tools. It emphasizes the practical issues faced by the semiconductor design engineer in terms of synthesis and the integration of front-end and back-end tools. Traditional design methodologies are challenged and unique solutions are offered to help define the next generation of ASIC design flows. The author provides numerous practical examples derived from real-world situations that will prove valuable to practicing ASIC design engineers as well as to students of advanced VLSI courses in ASIC design'. Dr Dwight W. Decker, Chairman and CEO, Conexant Systems, Inc., (Formerly, Rockwell

Semiconductor Systems), Newport Beach, CA, USA.

Languages for Digital Embedded Systems

The Designer's Guide to Verilog-AMS

Appropriate for use as a graduate text or a professional reference, Languages for Digital Embedded Systems is the first detailed, broad survey of hardware and software description languages for embedded system design. Instead of promoting the one language that will solve all design problems (which does not and will not ever exist), this book takes the view that different problems demand different languages, and a designer who knows the spectrum of available languages has the advantage over one who is trapped using the wrong language. Languages for Digital Embedded Systems concentrates on successful, widely-used design languages, with a secondary emphasis on those with significant theoretical value. The syntax, semantics, and implementation of each language is discussed, since although hardware synthesis and software compilation technology have steadily improved, coding style still matters, and a thorough understanding of how a language is synthesized or compiled is generally necessary to take full advantage of a language. Practicing designers, graduate students, and advanced undergraduates will all benefit from this book. It assumes familiarity with some hardware or software languages, but takes a

practical, descriptive view that avoids formalism.

Constraining Designs for Synthesis and Timing Analysis

Conventional computational methods, and even the latest soft computing paradigms, often fall short in their ability to offer solutions to many real-world problems due to uncertainty, imprecision, and circumstantial data. Hybrid intelligent computing is a paradigm that addresses these issues to a considerable extent. The Handbook of Research on Advanced Hybrid Intelligent Techniques and Applications highlights the latest research on various issues relating to the hybridization of artificial intelligence, practical applications, and best methods for implementation. Focusing on key interdisciplinary computational intelligence research dealing with soft computing techniques, pattern mining, data analysis, and computer vision, this book is relevant to the research needs of academics, IT specialists, and graduate-level students.

Twelfth International Conference on VLSI Design

Presenting a comprehensive overview of the design automation algorithms, tools, and methodologies used to design integrated circuits, the Electronic Design Automation for Integrated Circuits Handbook is available in two volumes. The second volume, EDA for IC Implementation, Circuit Design, and Process Technology, thoroughly examines real-time logic to

GDSII (a file format used to transfer data of semiconductor physical layout), analog/mixed signal design, physical verification, and technology CAD (TCAD). Chapters contributed by leading experts authoritatively discuss design for manufacturability at the nanoscale, power supply network design and analysis, design modeling, and much more. Save on the complete set.

Electronic Design

This book constitutes the proceedings of the 9th Workshop on RFID Security and Privacy, RFIDsec 2013, held in Graz, Austria, in July 2013. The 11 papers presented in this volume were carefully reviewed and selected from 23 submissions. RFIDsec deals with topics of importance to improving the security and privacy of RFID, NFC, contactless technologies, and the Internet of Things. RFIDsec bridges the gap between cryptographic researchers and RFID developers.

SystemVerilog for Verification

Advanced ASIC Chip Synthesis: Using Synopsys® Design Compiler® Physical Compiler® and PrimeTime®, Second Edition describes the advanced concepts and techniques used towards ASIC chip synthesis, physical synthesis, formal verification and static timing analysis, using the Synopsys suite of tools. In addition, the entire ASIC design flow methodology targeted for VDSM (Very-Deep-Sub-Micron) technologies is covered in detail. The

emphasis of this book is on real-time application of Synopsys tools, used to combat various problems seen at VDSM geometries. Readers will be exposed to an effective design methodology for handling complex, sub-micron ASIC designs. Significance is placed on HDL coding styles, synthesis and optimization, dynamic simulation, formal verification, DFT scan insertion, links to layout, physical synthesis, and static timing analysis. At each step, problems related to each phase of the design flow are identified, with solutions and work-around described in detail. In addition, crucial issues related to layout, which includes clock tree synthesis and back-end integration (links to layout) are also discussed at length. Furthermore, the book contains in-depth discussions on the basis of Synopsys technology libraries and HDL coding styles, targeted towards optimal synthesis solution. Target audiences for this book are practicing ASIC design engineers and masters level students undertaking advanced VLSI courses on ASIC chip design and DFT techniques.

Handbook of Research on Advanced Hybrid Intelligent Techniques and Applications

Logic synthesis has become a fundamental component of the ASIC design flow, and Logic Synthesis Using Synopsys® has been written for all those who dislike reading manuals but who still like to learn logic synthesis as practised in the real world. The primary focus of the book is Synopsys Design Compiler®: the leading synthesis tool in the EDA

marketplace. The book is specially organized to assist designers accustomed to schematic capture based design to develop the required expertise to effectively use the Compiler. Over 100 `classic scenarios' faced by designers using the Design Compiler have been captured and discussed, and solutions provided. The scenarios are based both on personal experiences and actual user queries. A general understanding of the problem-solving techniques provided will help the reader debug similar and more complicated problems. Furthermore, several examples and dc-shell scripts are provided. Specifically, Logic Synthesis Using Synopsys® will help the reader develop a better understanding of the synthesis design flow, optimization strategies using the Design Compiler, test insertion using the Test Compiler®, commonly used interface formats such as EDIF and SDF, and design re-use in a synthesis-based design methodology. Examples have been provided in both VHDL and Verilog. Audience: Written with CAD engineers in mind to enable them to formulate an effective synthesis-based ASIC design methodology. Will also assist design teams to better incorporate and effectively integrate synthesis with their existing in-house design methodology and CAD tools.

Tcl and the Tk Toolkit

This book offers an in-depth study of the design and challenges addressed by a high-level synthesis tool targeting a specific class of cryptographic kernels, i.e. symmetric key cryptography. With the aid of detailed case studies, it also discusses optimization strategies

that cannot be automatically undertaken by CRYKET (Cryptographic kernels toolkit. The dynamic nature of cryptography, where newer cryptographic functions and attacks frequently surface, means that such a tool can help cryptographers expedite the very large scale integration (VLSI) design cycle by rapidly exploring various design alternatives before reaching an optimal design option. Features include flexibility in cryptographic processors to support emerging cryptanalytic schemes; area-efficient multinational designs supporting various cryptographic functions; and design scalability on modern graphics processing units (GPUs). These case studies serve as a guide to cryptographers exploring the design of efficient cryptographic implementations.

MIPS Microprocessor Simulation Using Cadence NC-Verilog Simulation Environment

Verilog HDL

Presents a thorough introduction to VHDL programming, stressing a variety of programming methods for solving design problems--each of which includes extensive examples to illustrate principles as well as advanced concepts of VHDL programming. Covers such specialized topics as interfacing VHDL to C and concurrent simulations. Real-world, SOTA examples, simulations of microprocessors and their associate ``glue'' chips are also included.

Verification Methodology Manual for SystemVerilog

This book describes in detail all required technologies and methodologies needed to create a comprehensive, functional design verification strategy and environment to tackle the toughest job of guaranteeing first-pass working silicon. The author first outlines all of the verification sub-fields at a high level, with just enough depth to allow an engineer to grasp the field before delving into its detail. He then describes in detail industry standard technologies such as UVM (Universal Verification Methodology), SVA (SystemVerilog Assertions), SFC (SystemVerilog Functional Coverage), CDV (Coverage Driven Verification), Low Power Verification (Unified Power Format UPF), AMS (Analog Mixed Signal) verification, Virtual Platform TLM2.0/ESL (Electronic System Level) methodology, Static Formal Verification, Logic Equivalency Check (LEC), Hardware Acceleration, Hardware Emulation, Hardware/Software Co-verification, Power Performance Area (PPA) analysis on a virtual platform, Reuse Methodology from Algorithm/ESL to RTL, and other overall methodologies.

The Design Warrior's Guide to FPGAs

This is the first book to cover verification strategies and methodologies for SOC verification from system level verification to the design sign-off. All the verification aspects in this exciting new book are illustrated with a single reference design for Bluetooth

application.

EDN

Offers users the first resource guide that combines both the methodology and basics of SystemVerilog Addresses how all these pieces fit together and how they should be used to verify complex chips rapidly and thoroughly. Unique in its broad coverage of SystemVerilog, advanced functional verification, and the combination of the two.

ASIC/SoC Functional Design Verification

The Verilog Hardware Description Language (Verilog-HDL) has long been the most popular language for describing complex digital hardware. It started life as a prop- etary language but was donated by Cadence Design Systems to the design community to serve as the basis of an open standard. That standard was formalized in 1995 by the IEEE in standard 1364-1995. About that same time a group named Analog Verilog International formed with the intent of proposing extensions to Verilog to support analog and mixed-signal simulation. The first fruits of the labor of that group became available in 1996 when the language definition of Verilog-A was released. Verilog-A was not intended to work directly with Verilog-HDL. Rather it was a language with Similar syntax and related semantics that was intended to model analog systems and be compatible with SPICE-class circuit simulation engines. The first implementation of Verilog-A soon followed: a version from Cadence that

ran on their Spectre circuit simulator. As more implementations of Verilog-A became available, the group defining the a- log and mixed-signal extensions to Verilog continued their work, releasing the defi- tion of Verilog-AMS in 2000. Verilog-AMS combines both Verilog-HDL and Verilog-A, and adds additional mixed-signal constructs, providing a hardware description language suitable for analog, digital, and mixed-signal systems. Again, Cadence was first to release an implementation of this new language, in a product named AMS Designer that combines their Verilog and Spectre simulation engines.

Verilog — 2001

Functional Design Errors in Digital Circuits Diagnosis covers a wide spectrum of innovative methods to automate the debugging process throughout the design flow: from Register-Transfer Level (RTL) all the way to the silicon die. In particular, this book describes: (1) techniques for bug trace minimization that simplify debugging; (2) an RTL error diagnosis method that identifies the root cause of errors directly; (3) a counterexample-guided error-repair framework to automatically fix errors in gate-level and RTL designs; (4) a symmetry-based rewiring technology for fixing electrical errors; (5) an incremental verification system for physical synthesis; and (6) an integrated framework for post-silicon debugging and layout repair. The solutions provided in this book can greatly reduce debugging effort, enhance design quality, and ultimately enable the design and manufacture of more reliable electronic

devices.

Electronic Business

Reuse Methodology Manual

This book makes powerful Field Programmable Gate Array (FPGA) and reconfigurable technology accessible to software engineers by covering different state-of-the-art high-level synthesis approaches (e.g., OpenCL and several C-to-gates compilers). It introduces FPGA technology, its programming model, and how various applications can be implemented on FPGAs without going through low-level hardware design phases. Readers will get a realistic sense for problems that are suited for FPGAs and how to implement them from a software designer's point of view. The authors demonstrate that FPGAs and their programming model reflect the needs of stream processing problems much better than traditional CPU or GPU architectures, making them well-suited for a wide variety of systems, from embedded systems performing sensor processing to large setups for Big Data number crunching. This book serves as an invaluable tool for software designers and FPGA design engineers who are interested in high design productivity through behavioural synthesis, domain-specific compilation, and FPGA overlays. Introduces FPGA technology to software developers by giving an overview of FPGA programming models and design tools, as well as various application examples; Provides a holistic analysis of the topic and enables

developers to tackle the architectural needs for Big Data processing with FPGAs; Explains the reasons for the energy efficiency and performance benefits of FPGA processing; Provides a user-oriented approach and a sense for where and how to apply FPGA technology.

Energy-Efficient Communication Processors

Synthesis Methodology for Built-in At-speed Testing

VERILOG HDL, Second Editionby Samir PalnitkarWith a Foreword by Prabhu GoelWritten forboth experienced and new users, this book gives you broad coverage of VerilogHDL. The book stresses the practical design and verification perspective ofVerilog rather than emphasizing only the language aspects. The informationpresented is fully compliant with the IEEE 1364-2001 Verilog HDL standard. Among its many features, this edition- bull; bull;Describes state-of-the-art verification methodologies bull;Provides full coverage of gate, dataflow (RTL), behavioral and switch modeling bull;Introduces you to the Programming Language Interface (PLI) bull;Describes logic synthesis methodologies bull;Explains timing and delay simulation bull;Discusses user-defined primitives bull;Offers many practical modeling tips Includes over 300 illustrations, examples, and exercises, and a Verilog resource list.Learning objectives and summaries are provided for each

chapter. About the CD-ROMThe CD-ROM contains a Verilog simulator with agraphical user interface and the source code for the examples in the book. Whatpeople are saying about Verilog HDL- "Mr.Palnitkar illustrates how and why Verilog HDL is used to develop today'smost complex digital designs. This book is valuable to both the novice and theexperienced Verilog user. I highly recommend it to anyone exploring Verilogbased design." -RajeevMadhavan, Chairman and CEO, Magma Design Automation "Thisbook is unique in its breadth of information on Verilog and Verilog-relatedtopics. It is fully compliant with the IEEE 1364-2001 standard, contains allthe information that you need on the basics, and devotes several chapters toadvanced topics such as verification, PLI, synthesis and modelingtechniques." -MichaelMcNamara, Chair, IEEE 1364-2001 Verilog Standards Organization Thishas been my favorite Verilog book since I picked it up in college. It is theonly book that covers practical Verilog. A must have for beginners andexperts." -BerendOzceri, Design Engineer, Cisco Systems, Inc. "Simple,logical and well-organized material with plenty of illustrations, makes this anideal textbook." -Arun K. Somani, Jerry R. Junkins Chair Professor,Department of Electrical and Computer Engineering, Iowa State University, Ames PRENTICE HALL Professional Technical Reference Upper Saddle River, NJ 07458 www.phptr.com ISBN: 0-13-044911-3

17th IEEE VLSI Test Symposium

John K. Ousterhout’s Definitive Introduction to

Tcl/Tk–Now Fully Updated for Tcl/Tk 8.5 Tcl and the Tk Toolkit, Second Edition, is the fastest way for newcomers to master Tcl/Tk and is the most authoritative resource for experienced programmers seeking to gain from Tcl/Tk 8.5's powerful enhancements. Written by Tcl/Tk creator John K. Ousterhout and top Tcl/Tk trainer Ken Jones, this updated volume provides the same extraordinary clarity and careful organization that made the first edition the world's number one Tcl/Tk tutorial. Part I introduces Tcl/Tk through simple scripts that demonstrate its value and offer a flavor of the Tcl/Tk scripting experience. The authors then present detailed, practical guidance on every feature necessary to build effective, efficient production applications–including variables, expressions, strings, lists, dictionaries, control flow, procedures, namespaces, file and directory management, interprocess communication, error and exception handling, creating and using libraries, and more. Part II turns to the Tk extension and Tk 8.5's new themed widgets, showing how to organize sophisticated user interface elements into modern GUI applications for Tcl. Part III presents incomparable coverage of Tcl's C functions, which are used to create new commands and packages and to integrate Tcl with existing C software–thereby leveraging Tcl's simplicity while accessing C libraries or executing performance-intensive tasks. Throughout, the authors illuminate all of Tcl/Tk 8.5's newest, most powerful improvements. You'll learn how to use new Starkits and Starpacks to distribute run-time environments and applications through a single file; how to take full advantage of the new virtual file system support to treat entities such

as zip archives and HTTP sites as mountable file systems; and more. From basic syntax to simple Tcl commands, user interface development to C integration, this fully updated classic covers it all. Whether you're using Tcl/Tk to automate system/network administration, streamline testing, control hardware, or even build desktop or Web applications, this is the one Tcl/Tk book you'll always turn to for answers.

The ASIC Handbook

Logic Synthesis Using Synopsys®

This book constitutes the proceedings of the 2th International Workshop on Lightweight Cryptography for Security and Privacy, LightSec 2013, held in Gebze, Turkey, during May 6-7, 2013. The 10 full papers presented together with 3 invited talks were carefully reviewed and selected from 27 submissions. The papers are grouped in topical sections on efficient Implementations and designs, block cipher cryptanalysis, wireless sensor networks, and cryptographic protocols.

Advanced ASIC Chip Synthesis

Engineering productivity in integrated circuit product design and - velopment today is limited largely by the effectiveness of the CAD tools used. For those domains of product design that are highly dependent on transistor-level circuit design and optimization,

such as high-speed logic and memory, mixed-signal analog-digital int- faces, RF functions, power integrated circuits, and so forth, circuit simulation is perhaps the single most important tool. As the complexity and performance of integrated electronic systems has increased with scaling of technology feature size, the capabilities and sophistication of the underlying circuit simulation tools have correspondingly increased. The absolute size of circuits requiring transistor-level simulation has increased dramatically, creating not only problems of computing power resources but also problems of task organization, complexity management, output representation, initial condition setup, and so forth. Also, as circuits of more c- plexity and mixed types of functionality are attacked with simu- tion, the spread between time constants or event time scales within the circuit has tended to become wider, requiring new strategies in simulators to deal with large time constant spreads.

System-on-a-Chip Verification

Field Programmable Gate Arrays (FPGAs) are devices that provide a fast, low-cost way for embedded system designers to customize products and deliver new versions with upgraded features, because they can handle very complicated functions, and be reconfigured an infinite number of times. In addition to introducing the various architectural features available in the latest generation of FPGAs, The Design Warrior’s Guide to FPGAs also covers different design tools and flows. This book covers information

ranging from schematic-driven entry, through traditional HDL/RTL-based simulation and logic synthesis, all the way up to the current state-of-the-art in pure C/C++ design capture and synthesis technology. Also discussed are specialist areas such as mixed hardward/software and DSP-based design flows, along with innovative new devices such as field programmable node arrays (FPNAs). Clive "Max" Maxfield is a bestselling author and engineer with a large following in the electronic design automation (EDA)and embedded systems industry. In this comprehensive book, he covers all the issues of interest to designers working with, or contemplating a move to, FPGAs in their product designs. While other books cover fragments of FPGA technology or applications this is the first to focus exclusively and comprehensively on FPGA use for embedded systems. First book to focus exclusively and comprehensively on FPGA use in embedded designs World-renowned best-selling author Will help engineers get familiar and succeed with this new technology by providing much-needed advice on choosing the right FPGA for any design project

Advanced ASIC Chip Synthesis

PLEASE PROVIDE COURSE INFORMATION PLEASE PROVIDE

Functional Design Errors in Digital Circuits

by Phil Moorby The Verilog Hardware Description

Language has had an amazing impact on the mod em electronics industry, considering that the essential composition of the language was developed in a surprisingly short period of time, early in 1984. Since its introduc tion, Verilog has changed very little. Over time, users have requested many improve ments to meet new methodology needs. But, it is a complex and time consuming process to add features to a language without ambiguity, and maintaining consistency. A group of Verilog enthusiasts, the IEEE 1364 Verilog committee, have broken the Verilog feature doldrums. These individuals should be applauded. They invested the time and energy, often their personal time, to understand and resolve an extensive wish-list of language enhancements. They took on the task of choosing a feature set that would stand up to the scrutiny of the standardization process. I would like to per sonally thank this group. They have shown that it is possible to evolve Verilog, rather than having to completely start over with some revolutionary new language. The Verilog 1364-2001 standard provides many of the advanced building blocks that users have requested. The enhancements include key components for verification, abstract design, and other new methodology capabilities. As designers tackle advanced issues such as automated verification, system partitioning, etc., the Verilog standard will rise to meet the continuing challenge of electronics design.

VHDL Programming with Advanced Topics

The Designer's Guide to Spice and Spectre®

The aim of this project is to successfully complete ASIC design flow from RTL to GDSII using advanced industry-level tools. This project provides a solid base and practical hands-on experience of advanced tools like Cadence NC Simulator (Behavioral Simulation and Post Synthesis Simulation), Synopsys Design Compiler (Logic Synthesis), Synopsys DFT Compiler (Logic Scan Insertion and Boundary Scan Insertion), Synopsys Power Compiler (Power Optimization using clock gating), Synopsys Tetra Max (Determine Fault Coverage) and Synopsys IC Compiler (Design planning, Power Network Synthesis, Clock Tree Synthesis, Place and Route and Chip Finishing). The analysis of various design factors affecting the performance of the final chip such as power, area and timing is also performed.

Digital VLSI Chip Design with Cadence and Synopsys CAD Tools

XV From the Old to the New xvii Acknowledgments xx| Verilog A Tutorial Introduction Getting Started 2 A Structural Description 2 Simulating the binaryToESeg Driver 4 Creating Ports For the Module 7 Creating a Testbench For a Module 8 Behavioral Modeling of Combinational Circuits 11 Procedural Models 12 Rules for Synthesizing Combinational Circuits 13 Procedural Modeling of Clocked Sequential Circuits 14 Modeling Finite State Machines 15 Rules for Synthesizing Sequential Systems 18 Non-Blocking Assignment ("

Implementation of Asynchronous Interface ASIC Flow (RTL-to-GDSII) Using Cadence and Synopsys Tools

KEY BENEFIT: This hands-on book leads readers through the complete process of building a ready-to-fabricate CMOS integrated circuit using popular commercial design software. KEY TOPICS: The VLSI CAD flow described in this book uses tools from two vendors: Cadence Design Systems, Inc. and Synopsys Inc. Detailed tutorials include step-by-step instructions and screen shots of tool windows and dialog boxes. MARKET: A useful reference for chip designers.

FPGA

This book describes for readers a methodology for dynamic power estimation, using Transaction Level Modeling (TLM). The methodology exploits the existing tools for RTL simulation, design synthesis and SystemC prototyping to provide fast and accurate power estimation using Transaction Level Power Modeling (TLPM). Readers will benefit from this innovative way of evaluating power on a high level of abstraction, at an early stage of the product life cycle, decreasing the number of the expensive design iterations.

Radio Frequency Identification: Security and Privacy Issues

Based on the highly successful second edition, this

extended edition of SystemVerilog for Verification: A Guide to Learning the Testbench Language Features teaches all verification features of the SystemVerilog language, providing hundreds of examples to clearly explain the concepts and basic fundamentals. It contains materials for both the full-time verification engineer and the student learning this valuable skill. In the third edition, authors Chris Spear and Greg Tumbush start with how to verify a design, and then use that context to demonstrate the language features, including the advantages and disadvantages of different styles, allowing readers to choose between alternatives. This textbook contains end-of-chapter exercises designed to enhance students' understanding of the material. Other features of this revision include: New sections on static variables, print specifiers, and DPI from the 2009 IEEE language standard Descriptions of UVM features such as factories, the test registry, and the configuration database Expanded code samples and explanations Numerous samples that have been tested on the major SystemVerilog simulators SystemVerilog for Verification: A Guide to Learning the Testbench Language Features, Third Edition is suitable for use in a one-semester SystemVerilog course on SystemVerilog at the undergraduate or graduate level. Many of the improvements to this new edition were compiled through feedback provided from hundreds of readers.